REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

REV																					
PAGE																					
REV																					
PAGE																					
REV STATUS OF PAGES	**REV**																				
	PAGE	1	2	3	4	5	6	7	8	9	10	11	12								

PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 12-12-03	**CHECKED BY** Phu H. Nguyen **APPROVED BY** Thomas M. Hess	**TITLE** MICROCIRCUIT, DIGITAL, DSP MICROCOMPUTER, MONOLITHIC SILICON
	SIZE A **CODE IDENT. NO.** 16236	**DWG NO.** **V62/13601**
	REV	**PAGE** 1 **OF** 12

AMSC N/A

5962-V030-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance DSP microcomputer microcircuit, with an operating temperature range of -55°C to +110°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/13601	-	01	X	B
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	ADSP-21065L-EP	DSP Microcomputer

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	208	JEDEC MS-029	Metric Quad Flat Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage (V_{DD}) ..... -0.3 V to +4.6 V
Input voltage ..... -0.5 V to V_{DD} + 0.5 V
Output voltage Swing ..... -0.5 V to V_{DD} + 0.5 V
Load capacitance ..... 200 pF
Storage temperature range ..... -65°C to 150°C
Lead temperature (5 seconds) ..... 280°C
Junction temperature under bias ..... 150°C

1.4 Thermal characteristics.

This device is specified for a case temperature:

$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$ where:

T_{CASE} = Case temperature (measured on top surface of package)

PD = Power dissipation in W (This value depends upon the specific application)

θ_{JC} = 7.1°C/W

Case outline X			
Parameter	Airflow (Linear FT./Min)	Typical	Unit
θ_{CA}	0	24	°C/W
	100	20	
	200	19	
	400	17	
	600	13	

1.5 Operating conditions.

Supply voltage (V_{DD}) ..... 3.13 V to 3.60 V
High level input voltage @ V_{DD} = Max (V_{IH})..... 2.0 V to V_{DD} + 0.5 V
Low level input voltage @ V_{DD} = Max (V_{IL1}) ..... -0.5 V to 0.8 V 2/
Low level input voltage @ V_{DD} = Min (V_{IL2}) ..... -0.5 V to 0.7 V 3/
Case operating temperature (T_{CASE}) ..... -55°C to 110°C

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

2/ Applies to input and bidirectional pins: $DATA_{31-0}$, $ADDR_{23-0}$, BSEL, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{11-0}$, $\overline{HGB}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{2-1}$, $\overline{ID}_{2-0}$, RPBA, $\overline{CPA}$, TFS0, TFS1, RFS0, RFS1, $\overline{BMS}$, TMS, TDI, TCK, $\overline{HBR}$, DR0A, DR1A, DR0B, DR1B, TCLK0, TCLK1, RCLK0, RCLK1, $\overline{RESET}$, $\overline{TRST}$, PWM_EVENT0, PWM_EVENT1, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{SDCKE}$.

3/ Applies to input pin CLKIN.

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

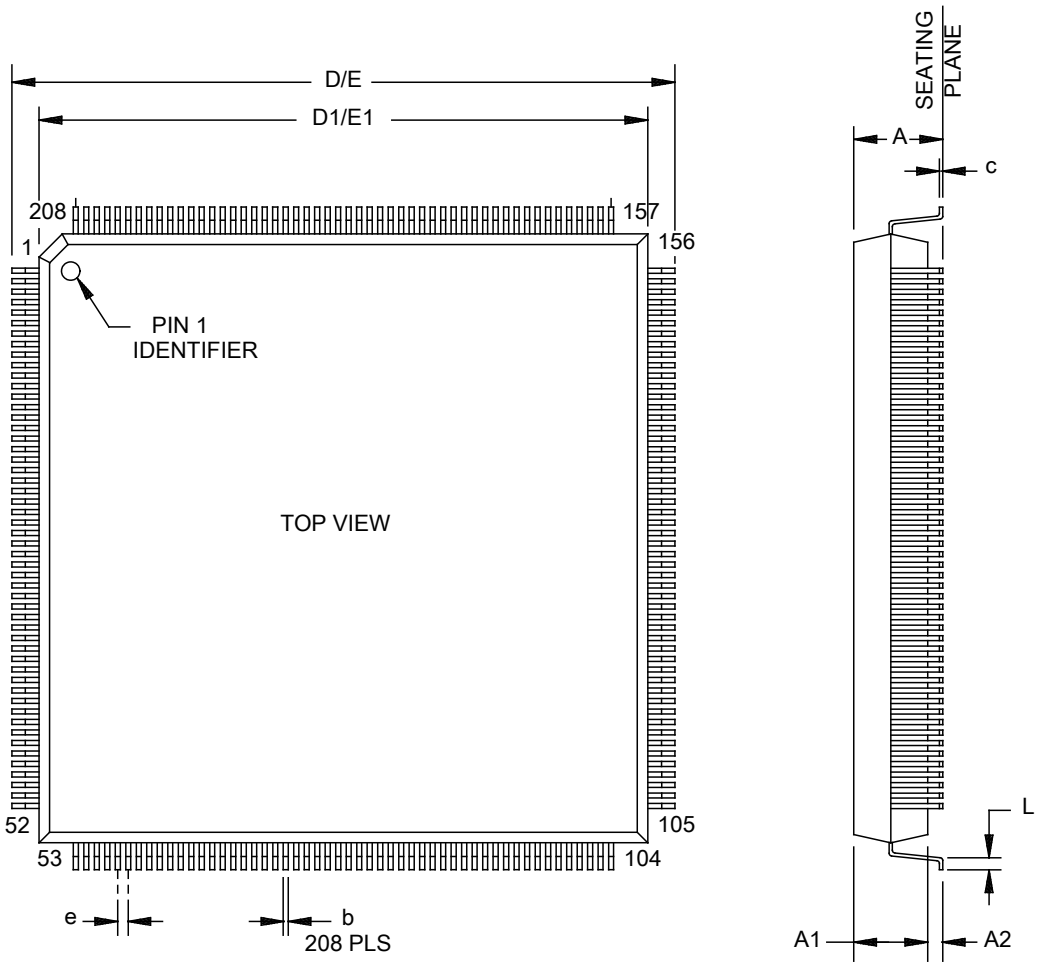
3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 Functional block diagram. The functional block diagram shall be as shown in figure 4.

Case X



Dimensions					
Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
A		4.10	D/E	30.35	30.85
A1	3.20	3.60	D1/E1	27.80	28.20
A2	0.25	0.50	e	0.50 BSC	
b	0.17	0.27	L	0.45	0.75
c	0.09	0.20			

NOTES:
1. The actual position of each lead is within 0.08 from its ideal position when measured in the lateral direction.
2. Center dimensions are nominal.
3. Dimensions are in millimeters and comply with JEDEC standard MS-029, FA-1.

FIGURE 1. Case outline.

Case outline X									
Terminal number	**Terminal symbol**	**Terminal number**	**Terminal symbol**	**Terminal number**	**Terminal symbol**	**Terminal number**	**Terminal symbol**	**Terminal number**	**Terminal symbol**
1	VDD	43	$\overline{\text{CAS}}$	85	VDD	127	DATA28	169	ADDR17
2	RFS0	44	$\overline{\text{SDWE}}$	86	DATA3	128	DATA29	170	ADDR16
3	GND	45	VDD	87	DATA4	129	GND	171	ADDR15
4	RCLK0	46	DQM	88	DATA5	130	VDD	172	VDD
5	DR0A	47	SDCKE	89	GND	131	VDD	173	ADDR14
6	DR0B	48	SDA10	90	DATA6	132	DATA30	174	ADDR13
7	TFS0	49	GND	91	DATA7	133	DATA31	175	ADDR12
8	TCLK0	50	$\overline{\text{DMAG}}1$	92	DATA8	134	FLAG7	176	VDD
9	VDD	51	$\overline{\text{DMAG}}2$	93	VDD	135	GND	177	GND
10	GND	52	$\overline{\text{HBG}}$	94	GND	136	FLAG6	178	ADDR11
11	DT0A	53	BMSTR	95	VDD	137	FLAG5	179	ADDR10
12	DT0B	54	VDD	96	DATA9	138	FLAG4	180	ADDR9
13	RFS1	55	$\overline{\text{CS}}$	97	DATA10	139	GND	181	GND
14	GND	56	$\overline{\text{SBTS}}$	98	DATA11	140	VDD	182	VDD
15	RCLK1	57	GND	99	GND	141	VDD	183	ADDR8
16	DR1A	58	$\overline{\text{WR}}$	100	DATA12	142	NC	184	ADDR7
17	DR1B	59	$\overline{\text{RD}}$	101	DATA13	143	ID1	185	ADDR6
18	TFS1	60	GND	102	NC	144	ID0	186	GND
19	TCLK1	61	VDD	103	NC	145	$\overline{\text{EMU}}$	187	GND
20	VDD	62	GND	104	DATA14	146	TDO	188	ADDR5
21	VDD	63	REDY	105	VDD	147	$\overline{\text{TRST}}$	189	ADDR4
22	DT1A	64	$\overline{\text{SW}}$	106	GND	148	TDI	190	ADDR3
23	DT1B	65	$\overline{\text{CPA}}$	107	DATA15	149	TMS	191	VDD
24	PWM_EVENT1	66	VDD	108	DATA16	150	GND	192	VDD
25	GND	67	VDD	109	DATA17	151	TCK	193	ADDR2
26	PWM_EVENT0	68	GND	110	VDD	152	BSEL	194	ADDR1
27	$\overline{\text{BR}}1$	69	ACK	111	DATA18	153	$\overline{\text{BMS}}$	195	ADDR0
28	$\overline{\text{BR}}2$	70	$\overline{\text{MS}}0$	112	DATA19	154	GND	196	GND
29	VDD	71	$\overline{\text{MS}}1$	113	DATA20	155	GND	197	FLAG0
30	CLKIN	72	GND	114	GND	156	VDD	198	FLAG1
31	XTAL	73	GND	115	NC	157	$\overline{\text{RESET}}$	199	FLAG2
32	VDD	74	$\overline{\text{MS}}2$	116	DATA21	158	VDD	200	VDD
33	GND	75	$\overline{\text{MS}}3$	117	DATA22	159	GND	201	FLAG3
34	SDCLK1	76	FLAG11	118	DATA23	160	ADDR23	202	NC
35	GND	77	VDD	119	GND	161	ADDR22	203	NC
36	VDD	78	FLAG10	120	VDD	162	ADDR21	204	GND
37	SDCLK0	79	FLAG9	121	DATA24	163	VDD	205	$\overline{\text{IRQ}}0$
38	$\overline{\text{DMAR}}1$	80	FLAG8	122	DATA25	164	ADDR20	206	$\overline{\text{IRQ}}1$
39	$\overline{\text{DMAR}}2$	81	GND	123	DATA26	165	ADDR19	207	$\overline{\text{IRQ}}2$
40	$\overline{\text{HBR}}$	82	DATA0	124	VDD	166	ADDR18	208	NC
41	GND	83	DATA1	125	GND	167	GND		
42	$\overline{\text{RAS}}$	84	DATA2	126	DATA27	168	GND		

FIGURE 2. Terminal connections.

Pin	Type 1/	Description
$ADDR_{23-0}$	I/O/T	**External Bus Address.** The ADSP-21065L-EP outputs addresses for external memory and peripherals on these pins. In a multiprocessor system, the bus master output addresses for read/writes of the IOP registers of the other ADSP-21065L-EP processors. The ADSP-21065L-EP inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$DATA_{31-0}$	I/O/T	**External Bus Data.** The ADSP-21065L-EP inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31-0. 16-bit short word data is transferred over bits 15-0 of the bus, Pull-up resistors on unused DATA pins are not necessary.
$\overline{MS}_{3-0}$	I/O/T	**Memory Select Lines.** These lines are asserted as chip selects for the corresponding banks of external memory. Internal $ADDR_{25-24}$ are decoded into $\overline{MS}_{3-0}$. The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{MS}_{3-0}$ line which is mapped to SDRAM may be asserted even when no SDRAM is active. In a multiprocessor system, the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{RD}$	I/O/T	**Memory Read Strobe.** This pin is asserted when the ADSP-21065L-EP reads from external memory devices or from the IOP register of another ADSP-21065L-EP. External devices (including another ADSP-21065L-EP) must assert $\overline{RD}$ to read from the ADSP-21065L-EP's IOP registers. In a multiprocessing system, $\overline{RD}$ is output by the bus master and is input by another ADSP-21065L-EP.
$\overline{WR}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L-EP writes to external memory devices or from the IOP register of another ADSP-21065L-EP. External devices must assert $\overline{WR}$ to write to the ADSP-21065L-EP's IOP registers. In a multiprocessing system, $\overline{WR}$ is output by the bus master and is input by the other ADSP-21065L-EP.
$\overline{SW}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L-EP to synchronous memory devices (including another ADSP-21065L-EP). The ADSP-21065L-EP asserts $\overline{SW}$ to provide an early an early indication of an impending write cycle, which can be aborted if $\overline{WR}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{SW}$ is output by the bus master and is input by the other ADSP-21065L-EP to determine if the multiprocessor access is a read or write. $\overline{SW}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge.** External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L-EP deasserts ACK as an output to add waitstates to a synchronous access of its IOP registers. In a multiprocessing system, a slave ADSP-21065L-EP deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{SBTS}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{SBTS}$ to place the external bus address, data, selects, and strobes – but not SDRAM control pins – in a high impedance state for the following cycle. If the ADSP-21065L-EP attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not finish until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from hose processor/ADSP-21065L-EP deadlock.
$\overline{IRQ}_{2-0}$	I/A	**Interrupt Request Lines.** May be either edge-triggered or level-sensitive.
$FLAG_{11-0}$	I/O/A	**Flag Pins.** Each is configured via control bits as either an input or output. As an input, they can be tested as a condition. As an output, they can be used to signal external peripherals.

See footnote at end of table.

FIGURE 3. Terminal function.

Pin	Type 1/	Description
$\overline{\text{HBR}}$	I/A	**Host Bus Request.** This pin must be asserted by a hose processor to request control of the ADSP-21065I-EP's external bus. When $\overline{\text{HBR}}$ is asserted in a multiprocessing system, the ADSP-21065I-EP that is a bus master will relinquish the bus and assert $\overline{\text{HBG}}$. To relinquish the bus, the ADSP-21065I-EP places the address, data, select, and strobe lines in a high impedance state. It does, however, continue to drive the SDRAM control pins. $\overline{\text{HBR}}$ has priority over all ADSP-21065I-EP bus requests (BR_{2-1}) in a multiprocessing system.
$\overline{\text{HBG}}$	I/O	**Host Bus Grant.** Acknowledges an $\overline{\text{HBR}}$ bus request, indicating that the host processor may take control of the external bus. $\overline{\text{HBG}}$ is asserted by the ADSP-21065L-EP until $\overline{\text{HBR}}$ is released. In a multiprocessing system, $\overline{\text{HBG}}$ is output by the ADSP-21065L-EP bus master.
$\overline{\text{CS}}$	I/A	**Chip Select.** Asserted by host processor to select the ADSP-21065L-EP.
REDY(O/D)	O	**Host Bus Acknowledge.** The ADSP-21065L-EP deasserts REDY to add wait states to an asynchronous access of its internal memory or IOP registers by a host. This pin is an open-drain output (O/D) by default; it can be programmed in the ADREDY bit of the SYSCON register to be active drive (A/D). REDY will only be output if the $\overline{\text{CS}}$ and $\overline{\text{HBR}}$ inputs are asserted.
$\overline{\text{DMAR}_1}$	I/A	**DMA Request 1** (DMA Channel 9).
$\overline{\text{DMAR}_2}$	I/A	**DMA Request 2** (DMA Channel 8).
$\overline{\text{DMAG}_1}$	O/T	**DMA Grant 1** (DMA Channel 9).
$\overline{\text{DMAG}_2}$	O/T	**DMA Grant 2** (DMA Channel 8).
$\overline{\text{BR}}_{2-1}$	I/O/S	**Multiprocessing Bus Requests.** Used by multiprocessing ADSP-21065L-EP processors to arbitrate for bus master-ship. An ADSP-21065L-EP only drives its own $\overline{\text{BR}}$x line (corresponding to the value of its ID_{2-0} inputs) and monitors all others. In a uniprocessor system, tie both $\overline{\text{BR}}$x pins to VDD.
ID_{1-0}	I	**Multiprocessing ID.** Determines which multiprocessor bus request ($\overline{\text{BR}}_1$-$\overline{\text{BR}}_2$) is used by the ADSP-21065L-EP. ID=01 corresponds to $\overline{\text{BR}}_1$, ID=10 corresponds to $\overline{\text{BR}}_2$, ID=00 in single-processor systems. These lines are a system configuration selection that should be hardwired or changed at reset only.
$\overline{\text{CPA}}$(O/D)	I/O	**Core Priority Access.** Asserting its $\overline{\text{CPA}}$ pin allows the core processor of an ADSP-21065L-EP bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{\text{CPA}}$ is an open-drain output that is connected to all ADSP-21065L-EP processors in the system. The $\overline{\text{CPA}}$ pin as an internal 5kΩ pull-up resistor. If core access priority is not required in a system, the $\overline{\text{CPA}}$ pin should be left unconnected.
DTxX	O	**Data Transmit (Serial Ports 0, 1; Channels A, B).** Each DTxX pin has a 50kΩ internal pull-up resistor.
DRxX	I	**Data Receive (Serial Ports 0, 1; Channels A, B).** Each DRxX pin has a 50kΩ pull-up resistor.
TLCKx	I/O	**Transmit Clock (Serial Ports 0, 1).** Each TCLK pin has a 50kΩ internal pull-up resistor.
RCLKx	I/O	**Receive Clock (Serial Ports 0, 1).** Each RCLK pin has a 50kΩ internal pull-up resistor.
TFSx	I/O	**Transmit Frame Sync (Serial Ports 0, 1).**
RFSx	I/O	**Receive Frame Sync (Serial Ports 0, 1).**

See footnote at end of table.

FIGURE 3. Terminal function - Continued.

Pin	Type 1/	Description
BSEL	I	**EPROM Boot Select.** When BSEL is high, the ADSP-21065L-EP is configured for booting from an 8-bit EPROM. When BSEL is low, the BSEL and $\overline{\text{BMS}}$ inputs determine booting mode. See $\overline{\text{BMS}}$ pin description below for details. This signal is a system configuration selection that should be hardwired.
$\overline{\text{BMS}}$	I/O/T*	**Boot Memory Select.** Output: Used as chip select for boot EPROM devices (when BSEL=1). In a multiprocessor system, BMS is output by the bus master. Input: When low, indicates that no booting will occur and that ADSP-21065L-EP will begin executing instructions from external memory. See table below. This input is a system configuration selection that should be hardwired. *Three-statable only in EPROM boot mode (when $\overline{\text{BMS}}$ is an output). **BSEL** **$\overline{\text{BMS}}$** **Booting Mode** 1 Output EPROM (connect $\overline{\text{BMS}}$ to EPROM chip select). 0 1 (Input) Host processor (HBW [SYSCON] bit selects host bus width). 0 0 (Input) No booting. Processor executes from external memory.
CLKIN	I	**Clock In.** Used in conjunction with XTAL, configures the ADSP-21065L-EP to use either its internal clock generator or an external clock source. The external crystal should be rated at 1x frequency. Connecting the necessary components to CLKIN and XTAL enables the internal clock generator. The ADSP-21065L-EP's internal clock generator multiplies the 1x clock to generate 2x clock for its core and SDRAM. It drives 2x clock out on the SDCLKx pins for the SDRAM interface to use. See also SDCLKx. Connecting the 1x external clock source. The instruction cycle rate is equal to 2x CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	**Processor Reset.** Resets the ADSP-21065L-EP to a known state and begin execution at the program memory location specified by the hardware reset vector address. This input must be asserted at power-up.
TCK	I	**Test Clock (JTAG).** Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	**Test Mode Select (JTAG).** Used to control the test state machine. TMS has a 20kΩ internal pull-up resistor.
TDI	I/S	**Test Data Input (JTAG).** Provides serial data for the boundary scan logic. TDI has a 20kΩ internal pull-up resistor.
TDO	O	**Test Data Output (JTAG).** Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	**Test Reset (JTAG).** Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21065L-EP. $\overline{\text{TRST}}$ has a 20kΩ internal pull-up resistor.
$\overline{\text{EMU}}$ (O/D)	O	**Emulation Status.** Must be connected to the ADSP-21065L-EP EZ-ICE target board connector only.
BMSTR	O	**Bus Master Output.** In a multiprocessor system, indicates whether the ADSP-21065L-EP is current bus master of the shared external bus. The ADSP-21065L-EP drives BMSTR high only while it is the bus master. In a single-processor system (ID=00), the processor drives this pin high.
$\overline{\text{CAS}}$	I/O/T	**SDRAM Column Access Strobe.** Provides the column address. In conjunction with $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
$\overline{\text{RAS}}$	I/O/T	**SDRAM Row Access Strobe.** Provides the row address. In conjunction with $\overline{\text{CAS}}$, $\overline{\text{MS}}$x, $\overline{\text{SDWE}}$, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.

See footnote at end of table.

FIGURE 3. Terminal function - Continued.

Case outline X - Continued

Pin	Type 1/	Description
$\overline{\text{SDWE}}$	I/O/T	**SDRAM Write Enable.** In conjunction with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, $\overline{\text{MS}}$x, SDCLKx, and sometimes SDA10, defines the operation for the SDRAM to perform.
DQM	O/T	**SDRAM Data Mask.** In write mode, DQM has a latency of zero and is used to block write operations.
$\text{SDCLK}_{1\text{-}0}$	I/O/S/T	**SDRAM2x Clock Output.** In systems with multiple SDRAM devices connected in parallel, supports the corresponding increased clock load requirements, eliminating need off off-chip clock buffers. Either SDCLK_1 or both SDCLKx pins can be three-stated.
SDCKE	I/O/T	**SDRAM Clock Enable.** Enables and disables the CLK signal. For details, see the data sheet supplied with your SDRAM device.
SDA10	O/T	**SDRAM A10 Pin.** Enables applications to refresh an SDRAM in parallel with a host access.
$\overline{\text{XTAL}}$	O	**Crystal Oscillator Terminal.** Used in conjunction with CLKIN to enable to ASDP-21065L-EP's internal clock generator or to disable it to use an external clock source. See CLKIN.
$\overline{\text{PWM\_EVENT}}_{1\text{-}0}$	I/O/A	**PWM Output/Event Capture.** In PWMOUT mode, is an output pin and functions as a timer counter. In WIDTH_CNT mode, is an input pin and functions as a pulse counter/event capture.
VDD	P	**Power Supply.** Nominally +3.3V dc. (33 pins)
GND	G	**Power Supply Return.** (37 pins)
NC		**Do Not Connect.** Reserved pins which must be left open and unconnected. (7 pins)

1. A = Asynchronous, G = Ground, I = Input, O = Output, P = Power supply, S = Synchronous, (A/D) = Active Drive, (O/D) = Open Drain, T = Three-State (when $\overline{\text{SBTS}}$ is asserted, or when then ADSP-21065L-EP is a bus slave).

FIGURE 3. Terminal function - Continued.

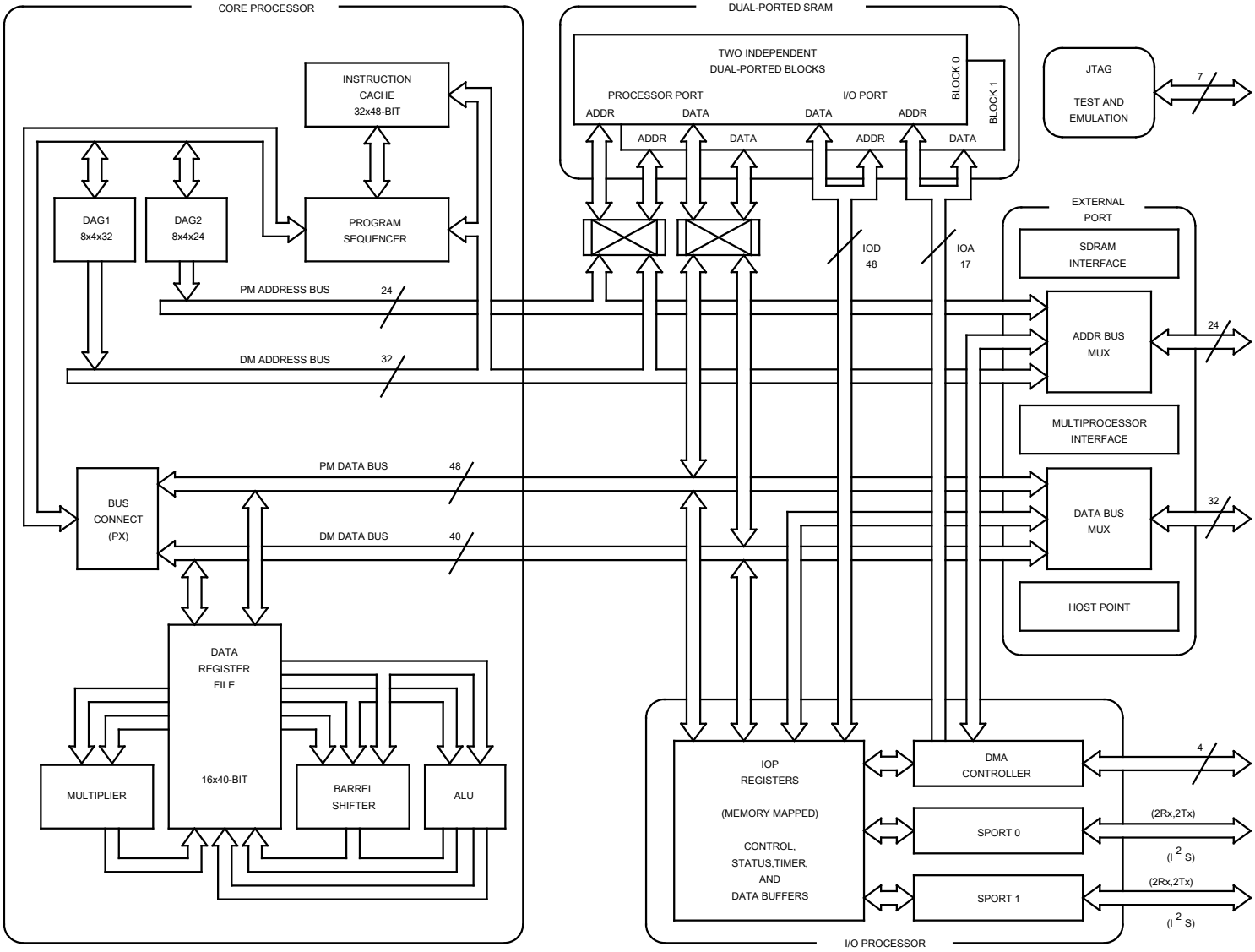


FIGURE 4. Functional block diagram.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/13601
		REV	PAGE 11

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/13601-01XB	24355	ADSP21065LSS240-EP

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106